WHAT IS CLAIMED IS:

1. A flash memory comprising:

a memory sector with a plurality of flash memory cells;

a command interface, which receives a write data input instruction from an external device, generates a write data input instruction signal, and receives a write instruction from the external device and generates a write instruction signal;

a first signal buffer, which receives a write enable signal input from the external device;

a control signal generation circuit, which is activated by the write instruction signal, and generates a control signal;

a data input buffer, which is activated by the write data input instruction signal to receive a write data input from the external device in synchronization with the write enable signal;

an error correction circuit, which is activated by the write data input instruction signal to receive the write data in synchronization with the write enable signal, and is activated by the write instruction signal to generate a check data for an error correction in synchronization with the control signal;

an address buffer, which receives an address data input from the external device;

an address signal generation circuit, which is

activated by the write data input instruction signal to generate an address signal in a predetermined order based on the address data in synchronization with the write enable signal, and is activated by the write instruction signal to generate an address signal in a predetermined order in synchronization with the control signal;

a plurality of data memory circuits, each of which is provided corresponding to each of said plurality of flash memory cells, and receives an allocated address signal, takes and temporarily memorizes the write data and the check data; and

means to be activated by the write instruction signal, and to write the write data and the check data, which are temporarily memorized in said plurality of data memory circuits in said memory sector.

2. The flash memory according to claim 1, further comprising a busy signal output circuit, which outputs a busy signal to the external device according to the write instruction signal.

3. A flash memory comprising:

a plurality of memory sectors, each of which has a plurality of flash memory cells;

a memory cell array having said plurality of memory sectors;

a control signal generation circuit, which generates a control signal;

a first signal buffer, which receives a read enable signal input from an external device;

an address buffer, which receives an address data input from the external device;

an address signal generation circuit, which generates an address signal in a predetermined order in synchronization with the control signal, and generates an address signal in a predetermined order based on the address data in synchronization with the read enable signal;

read means to select said memory sectors in said memory cell array based on the address data, and to read data from each of said plurality of flash memory cells of selected memory sectors;

a plurality of data memory circuits, each of which is provided for each of said plurality of flash memory cells, temporarily memorizes data read from said plurality of flash memory cells corresponding to selected memory sectors and receives an allocated address signal and outputs the data, which is temporarily memorized, read from said plurality of flash memory cells;

a data output buffer, which outputs the data, which is read from the said plurality of flash memory cells and output from said plurality of data memory circuits, to the external device in synchronization with the read enable signal; and

an error correction circuit, which receives the data, which is read from said plurality of flash memory cells and output from said plurality of data memory circuits, in synchronization with the control signal, judges whether the data output from the data output buffer has an error in synchronization with the read enable signal, and corrects an error if there is the error.

4. The flash memory according to claim 3, comprising a busy signal output circuit, which continuously outputs a busy signal to the external device for a period when data is read from the said plurality of flash memory cells and said error correction circuit receives data read from said plurality of flash memory cells.

5. The flash memory according to claim 3, further comprising:

a command interface, which receives the status read instruction from the external device to generate a status read instruction signal; and

status output means to be activated by the status read instruction signal to output whether there is an error in the data read from said plurality of flash memory cells through the data output buffer.

6. The flash memory according to claim 5, wherein said error correction circuit can correct a plurality of data in data read from said plurality of

flash memory cells, and

said status output means can output the number of errors.

7. The flash memory according to claim 5, wherein said error correction circuit can correct n data ($n \geqq 1$) in the data read from said plurality of flash memory cells and can detect an existence of (n+1) errors, and

said status output means can output whether the error can be corrected.

8. A flash memory comprising:

a plurality of memory sectors, each of which has a plurality of flash memory cells;

a memory cell array having said plurality of memory sectors;

a command interface, which receives a correction read instruction from an external device to generate a correction read instruction signal;

a control signal generation circuit, which is activated by the correction read instruction signal to generate a control signal;

a first signal buffer, which receives a read enable signal input from an external device;

an address buffer, which receives an address data input from the external device;

an address signal generation circuit, which generates an address signal in a predetermined order

based on the address data in synchronization with the read enable signal, and is activated by the correction read instruction signal to generate an address signal in a predetermined order in synchronization with the control signal;

read means to select said memory sectors in said memory cell array based on the address data, and to read data from each of said plurality of flash memory cells of selected memory sectors;

a plurality of data memory circuits, each of which is provided of each of said plurality of flash memory cells, temporarily memorizes a data read from said plurality of flash memory cells corresponding to the selected memory sector, respectively, receives an allocated address signal and outputs the data read from said plurality of flash memory cells, which is temporarily memorized;

a data output buffer, which outputs the data, which is read from the said plurality of flash memory cells and output from said plurality of data memory circuits, to the external device in synchronization with the read enable signal; and

an error correction circuit, which receives the data, which is read from said plurality of flash memory cells and output from said plurality of data memory circuits, in synchronization with the read enable signal, receives the data, which is read from said

plurality of flash memory cells and output from said plurality of data memory circuits, in synchronization with the control signal, judges whether there is an error in the data read from said plurality of flash memory cells, and specifies the data when there is an error.

9. The flash memory according to claim 8, wherein

the command interface receives a status read instruction signal and generates a status read instruction "70"H from the external device; and

status output means to output whether there is an error in the data which is activated by the status read instruction signal and read from said plurality of flash memory cells, through the data output buffer.

10. The flash memory according to claim 9, wherein

said error correction circuit can correct a plurality of data in data read from said plurality of flash memory cells, and

said status output means can output the number of errors.

11. The flash memory according to claim 9, wherein

said error correction circuit can correct n data ($n \geqq 1$) in the data read from said plurality of flash memory cells and can detect an existence of (n+1) errors, and

said status output means can output whether the error can be corrected.

12. The flash memory according to claim 8, further comprising a busy signal output circuit, which outputs a busy signal to the external device for reading period of data from the said plurality of flash memory cells, and outputs the busy signal to the external device and according to the correction read instruction signal.

13. A flash memory comprising:

a memory sector with a plurality of flash memory cells;

a command interface, which receives a write data input instruction from an external device to generate a write data input instruction signal, and receives a write instruction from the external device to generate a write instruction signal;

a first signal buffer, which receives a write enable signal input from the external device;

a control signal generation circuit, which is activated by the write instruction signal to generate a control signal;

a data input buffer, which is activated by the write data input instruction signal to receive a write data input from the external device in synchronization with the write enable signal;

an error correction circuit, which is activated by the write data input instruction signal to receive the write data in synchronization with the write enable signal, and is activated by the write instruction

signal to generate a check data for an error correction in synchronization with the control signal;

a plurality of data memory circuits, each of which is provided for each of said plurality of flash memory cells, and takes the write data and the check data in synchronization with the write enable signal and the control signal to memorize it temporarily; and

means to be activated by the write instruction signal, and to write the write data and the check data, which are temporarily memorized in said plurality of data memory circuits in said memory sector.

14. The flash memory according to claim 13, further comprising a busy signal output circuit, which outputs a busy signal to the external device according to the write instruction signal.

15. A flash memory comprising:

a plurality of memory sectors, each of which has a plurality of flash memory cells;

a memory cell array having said plurality of memory sectors;

a control signal generation circuit, which generates a control signal;

a first signal buffer, which receives a read enable signal input from an external device;

an address buffer, which receives an address data input from the external device;

read means to select said memory sectors in said

memory cell array based on the address data, and to read data from each of said plurality of flash memory cells of selected memory sectors;

a plurality of data memory circuits, each of which is provided for each of said plurality of flash memory cells, and temporarily memorizes the data read from said plurality of flash memory cells corresponding to said selected memory sector, and outputs the data read from said plurality of flash memory cells, which are temporarily memorized in synchronization with the control signal and the read enable signal;

a data output buffer, which outputs the data, which is read from said plurality of flash memory cells and output from said plurality of data memory circuits to the external device in synchronization with the read enable signal; and

an error correction circuit, which receives the data, which is read from said plurality of flash memory cells and output from said plurality of data memory circuits, in synchronization with the control signal, judges whether the data output from the data output buffer has an error in synchronization with the read enable signal, and corrects the error if there is an error.

16. The flash memory according to claim 15, comprising a busy signal output circuit, which continuously outputs a busy signal to the external

device for a period when data is read from the said plurality of flash memory cells and said error correction circuit receives data read from said plurality of flash memory cells.

17. The flash memory according to claim 15, further comprising:

a command interface, which receives the status read instruction from the external device to generate a status read instruction signal; and

status output means to be activated by the status read instruction signal to output whether there is an error in the data read from said plurality of flash memory cells through the data output buffer.

18. The flash memory according to claim 17, wherein

said error correction circuit can correct a plurality of data in data read from said plurality of flash memory cells, and

said status output means can output the number of errors.

19. The flash memory according to claim 17, wherein

said error correction circuit can correct n data ($n \geqq 1$) in the data read from said plurality of flash memory cells and can detect an existence of (n+1) errors, and

said status output means can output whether the

error can be corrected.

20. A flash memory comprising:

a plurality of memory sectors, each of which has a plurality of flash memory cells;

a memory cell array having said plurality of memory sectors;

a command interface, which receives a correction read instruction from an external device to generate a correction read instruction signal;

a control signal generation circuit, which is activated by the correction read instruction signal to generate a control signal;

a first signal buffer, which receives a read enable signal input from an external device;

an address buffer, which receives an address data input from the external device;

read means to select said memory sectors in said memory cell array based on the address data, and to read data from each of said plurality of flash memory cells of selected memory sectors;

a plurality of data memory circuits, each of which is provided for each of said plurality of flash memory cells, and temporarily memorizes the data read from said plurality of flash memory cells corresponding to said selected memory sector and outputs the data read from said plurality of flash memory cells which has been temporarily memorized in synchronization with the

read enable signal and the control signal;

a data output buffer, which outputs the data, which is read from the said plurality of flash memory cells and output from said plurality of data memory circuits, to the external device in synchronization with the read enable signal; and

an error correction circuit, which receives the data, which is read from said plurality of flash memory cells and output from said plurality of data memory circuits, in synchronization with the read enable signal, receives the data, which is read from said plurality of flash memory cells and output from said plurality of data memory circuits, in synchronization with the control signal, judges whether there is an error in the data read from said plurality of flash memory cells, and specifies the data when there is an error.

21. The flash memory according to claim 20, wherein

the command interface receives a status read instruction signal and generates a status read instruction "70"H from the external device; and

status output means to output whether there is an error in the data which is activated by the status read instruction signal and read from said plurality of flash memory cells, through the data output buffer.

22. The flash memory according to claim 21,

wherein

said error correction circuit can correct a plurality of data in data read from said plurality of flash memory cells, and

said status output means can output the number of errors.

23. The flash memory according to claim 21, wherein

said error correction circuit can correct n data ($n \geqq 1$) in the data read from said plurality of flash memory cells and can detect an existence of (n+1) errors, and

said status output means can output whether the error can be corrected.

24. The flash memory according to claim 20, further comprising a busy signal output circuit, which outputs a busy signal to the external device for reading period of data from the said plurality of flash memory cells, and outputs the busy signal to the external device and according to the correction read instruction signal.

25. A flash memory comprising:

a memory sector with a plurality of flash memory cells;

a signal buffer, which receives a write enable signal input from an external device, and outputs a first control signal in a first period;

data, which is read from said plurality of flash memory cells and output from said plurality of data memory circuits, in synchronization with the first control signal, judges whether the data output from the data output buffer has an error in synchronization with the second the signal, and corrects the error if there is an error.

28. The flash memory according to claim 27, comprising a busy signal output circuit, which continuously outputs a busy signal to the external device for a period when data is read from the said plurality of flash memory cells and said error correction circuit receives data read from said plurality of flash memory cells.

29. The flash memory according to claim 27, further comprising:

a command interface, which receives the status read instruction from the external device to generate a status read instruction signal; and

status output means to be activated by the status read instruction signal to output whether there is an error in the data read from said plurality of flash memory cells through the data output buffer.

30. The flash memory according to claim 29, wherein

said error correction circuit can correct a plurality of data in data read from said plurality of

a control signal generation circuit, which generates a second control signal in a second period different from the first period;

a data input buffer, which receives a write data input from the external device in synchronization with the write enable signal;

an error correction circuit, which receives the write data in synchronization with the first control signal, and generates a check data for an error correction in synchronization with the second control signal;

a plurality of data memory circuits, each of which is provided for each of said plurality of flash memory cells, and takes the write data and the check data in synchronization with the first control signal and the second control signal and memorizes it temporarily;

means to write the write data and the check data, which are temporarily memorized in said plurality of data memory circuits, in said memory sector.

26. The flash memory according to claim 25, further comprising a busy signal output circuit, which outputs busy signal to the external device in the second the period.

27. A flash memory comprising:

a plurality of memory sectors, each of which has a plurality of flash memory cells;

a memory cell array having said plurality of

memory sectors;

a control signal generation circuit, which generates a first control signal in a first period;

signal buffer, which receives a read enable signal input from an external device, and outputs a second control signal in a second period different from the first period;

an address buffer, which receives an address data input from the external device;

read means to select said memory sectors in said memory cell array based on the address data, and to read data from each of said plurality of flash memory cells of selected memory sectors;

a plurality of data memory circuits, each of which is provided for each of said plurality of flash memory cells, and temporarily memorizes the data read from said plurality of flash memory cells corresponding to said selected memory sector and outputs the data read from the memory cell, which temporarily memorizes it, in synchronization with the first control signal and the second control signal;

a data output buffer, which outputs the data, which is read from said plurality of flash memory cells and output from said plurality of data memory circuits, to the external device in synchronization with the second the signal;

an error correction circuit, which receives the

flash memory cells, and

said status output means can output the number of errors.

31. The flash memory according to claim 29, wherein

said error correction circuit can correct n data ($n \geqq 1$) in the data read from said plurality of flash memory cells and can detect an existence of (n+1) errors, and

said status output means can output whether the error can be corrected.

32. A flash memory comprising:

a plurality of memory sectors, each of which has a plurality of flash memory cells;

a memory cell array having said plurality of memory sectors;

a signal buffer, which receives a read enable signal input from an external device, and outputs a first control signal in a first period;

a control signal generation circuit, which generates a second control signal in a second period different from the first period;

an address buffer, which receives the address data input from the external device;

read means to select said memory sectors in said memory cell array based on the address data, and to read data from each of said plurality of flash memory

cells of selected memory sectors;

a plurality of data memory circuits, each of which is provided for each of said plurality of flash memory cells, temporarily memorizes the data read from said plurality of flash memory cells corresponding to said selected memory sector and outputs the data read from the memory cell, which temporarily memorizes it, in synchronization with the first control signal and the second control signal;

a data output buffer, which outputs the data, which is read from said plurality of flash memory cells and output from said plurality of data memory circuits, to the external device in synchronization with the first control signal;

an error correction circuit, which receives the data, which is read from said plurality of flash memory cells and output from said plurality of data memory circuits, in synchronization with the first control signal, receives the data, which is read from said plurality of flash memory cells and output from said plurality of data memory circuits, in synchronization with the second control signal, judges whether there is an error in the data read from said plurality of flash memory cells, and specifies the data when there is an error.

33. The flash memory according to claim 32, further comprising:

a command interface, which receives the status read instruction from the external device to generate a status read instruction signal; and

status output means to be activated by the status read instruction signal to output whether there is an error in the data read from said plurality of flash memory cells through the data output buffer.

34. The flash memory according to claim 33, wherein

said error correction circuit can correct a plurality of data in data read from said plurality of flash memory cells, and

said status output means can output the number of errors.

35. The flash memory according to claim 33, wherein

said error correction circuit can correct n data ($n \geqq 1$) in the data read from said plurality of flash memory cells and can detect an existence of (n+1) errors, and

said status output means can output whether the error can be corrected.

36. The flash memory according to claim 32, further comprising a busy signal output circuit which outputs busy signal to the external device in a read period of data from the memory cell, and outputs a busy signal to the external device in the second period.

37. A flash memory comprising:

a memory sector with a plurality of flash memory cells;

a busy signal output circuit, which outputs busy signal to the external device;

a data input buffer, which receives the write data written in each memory cell input from the external device;

a plurality of data memory circuits which can memorize n bits to temporarily memorize the write data; and

an error correction circuit, which takes m1-bits write data ($m1 < n$) to generates m2-bits check data, and takes m3 bits write data ($m1 + m2 + m3 < n$) to generate m4 bits check data ($m1 + m2 + m3 + m4 \leqq n$) after generating m2-bits check data ($m1 + m2 < n$), wherein

the m2-bits check data is input to said plurality of data memory circuits after the m1-bits write data is input to said plurality of data memory circuits to be memorized temporarily, the m4 bits check data is input to said plurality of data memory circuits after the m3 bits write data is input to said plurality of data memory circuits to be memorized temporarily, and the m1 and m3 bits write data and m2 and the m4 bits check data, which are temporarily memorized in said plurality of data memory circuits, are written in said memory

sector after the m4 bits check data is temporarily memorized in said plurality of data memory circuits.

when said error correction circuit generates the m2-bits check data, a busy signal is output from said busy signal output circuit to the external device.

38. A flash memory comprising:

a memory sector with a plurality of flash memory cells;

a busy signal output circuit, which outputs busy signal to the external device;

an error correction circuit, which reads the read data from said memory sector and specifies the error read data, wherein

a busy signal is continuously output from the busy signal output circuit to the external device from a period when the read data from said memory sector to a period when said error correction circuit specifies a error read data.

39. A flash memory comprising:

a memory sector with a plurality of flash memory cells;

a data buffer, which outputs a read data read from said memory sector to an external device;

an error correction circuit, which output the read data from the data buffer and inputs the read data to specify an error read data from the read data, wherein

when the read data is output from said data buffer

to the external device again, said error correction circuit corrects the error read data.

40. The flash memory according to claim 39, further comprising a status output circuit which outputs an error state to the external device.

41. The flash memory according to claim 39, further comprising a plurality of data memory circuits, which temporarily memorize to read data read from said memory sector.

42. A flash memory comprising:

a memory sector to which has a plurality of said plurality of flash memory cells;

means to write an information data and a check data in said memory sector;

means to read the information data and the check data from said memory sector; and

an error correction circuit, which generates the check data from the information data and performs an error correction of the information data based on the information data and the check data, wherein

said error correction circuit generate the check data by replacing the information data read from at least one predetermined memory cell with a predetermined dummy data, and corrects the information data by replacing the information data read from said predetermined memory cell with the dummy data.

43. A flash memory comprising:

a memory sector to which has a plurality of said plurality of flash memory cells;

means to write the predetermined n bits information data and a check data in said memory sector;

means to read the n bits information data and the check data from said memory sector; and

a error correction circuit, which generates the check data from the n bits information data and performs an error correction of the n bits information data from the n bits information data and the check data, wherein

said error correction circuit effectively adds a predetermined (n - m) bits dummy data as information data when the information data input from the external device is m bits (m < n), and generates the check data.

44. A flash memory comprising:

a memory sector to which has a plurality of said plurality of flash memory cells;

means to write an information data and a check data in said memory sector;

means to read the information data and the check data from said memory sector;

an error correction circuit, which generates the check data from the information data, and performs an error correction of the information data from the information data and the check data; and

a switch circuit, which selects whether the information data is output to the external device by performing the error correction or the information data is output to the external device without the error correction.

45. A flash memory comprising:

a memory sector to which has a plurality of said plurality of flash memory cells;

means to write an information data and a check data in said memory sector;

means to read the information data and the check data from said memory sector;

an error correction circuit, which generates the check data from the information data, and the error correction of the information data from the information data and the check data; and

a switch circuit, which selects whether said error correction circuit is activated or deactivated.

46. A flash memory comprising:

a plurality of memory sectors, each of which has a plurality of flash memory cells;

a memory cell array having said plurality of memory sectors;

means to write an information data and a check data in said memory sector;

means to read the information data and the check data from said memory sector;

an error correction circuit, which generates the check data from the information data, and the error correction of the information data from the information data and the check data; and

means to read data of a predetermined memory sector according to a turn-on of a power supply.

47. A flash memory comprising:

a memory sector to which has a plurality of said plurality of flash memory cells;

multi-level write means to write a first information data and a first check data in each of said plurality of flash memory cells of said memory sector per one bit, thereafter, further write one bit in each of said plurality of flash memory cells of said memory sector based on the written first information data, the written first check data, a second information data and second check, to write two-bits data in one memory cell;

multi-level read means to read the first information data and the first check data from said memory sector, and to read the second information data and the second check data from said memory sector; and

an error correction circuit, which generates the first check data from the first information data, generates the second check data from the second information data, corrects an error in the first information data from the first information data and

the first check data and corrects an error in the second information data from the second information data and the second check data, wherein

a said error correction circuit performs a generation and an error correction of the check data based on a BCH code.

48. A flash memory comprising:

a memory sector to which has a plurality of said plurality of flash memory cells;

an erase circuit which erases said memory sector, and sets data of all memory cells to "1";

means to write an information data and a check data in said memory sector;

means to read the information data and the check data from said memory sector; and

an error correction circuit, which generates the check data from the information data, and performs an error correction of the information data from the information data and the check data, wherein

said error correction circuit generates the check data of all "1" from the information data of all "1".

49. A flash memory comprising:

a memory sector with a plurality of flash memory cells;

an error correction circuit, which generates a check data for the error correction from an information data input from an external device, and performs

an error correction of the information data from the information data and the check data;

a plurality of data memory circuits each of which is provided to each of said plurality of flash memory cells;

means to write the information data and the check data, which are temporarily memorized in said plurality of data memory circuits, in said memory sector;

means to read the information data and the check data from said memory sector to said plurality of data memory circuits; and

means to output the information data and the check data, which is memorized in said plurality of data memory circuits, read from a memory sector to the external device.

50. A flash memory comprising:

a memory sector with a plurality of flash memory cells;

an error correction circuit, which generates a check data for the error correction from an information data input from an external device, and performs an error correction of the information data from the information data and the check data;

a plurality of data memory circuits each of which is provided to each of said plurality of flash memory cells;

means to write the information data and the check

data, which are temporarily memorized in said plurality of data memory circuits, in said memory sector; and

means to read the information data and the check data from said memory sector to said plurality of data memory circuits, wherein

the data memorized in said plurality of data memory circuits is reset to data predetermined "1" before inputting the information data from the external device.